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APPLICATION NUMBER: *60/456,775*
FILING DATE: *March 21, 2003*
RELATED PCT APPLICATION NUMBER: *PCT/US04/08724*

By Authority of the
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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EV281802265US

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Mark Alan LaMonte	Johnson	Raleigh, NC
Douglas William	Barlage	Raleigh, NC

☐ *Additional inventors are being named on the _____ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

NANOSCALE PATTERNING BY MULTIPERIOD EDGE DEFINITION (SPACER GATE) LITHOGRAPHY FOR ELECTRONIC, PHOTONIC, MOLECULAR-ELECTRONIC, SPINTRONIC AND OTHER NANOTECHNOLOGY APPLICATIONS

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ENCLOSED APPLICATION PARTS (check all that apply)

☒ Specification *Number of Pages*	15	☐ CD(s), Number	
☐ Drawing(s) *Number of Sheets*		☐ Other (specify)	
☐ Application Data Sheet. See 37 CFR 1.76			

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

		FILING FEE AMOUNT ($)
☒	Applicant claims small entity status. See 37 CFR 1.27.	
☐	A check or money order is enclosed to cover the filing fees	
☒	The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 50-0426	80.00
☐	Payment by credit card. Form PTO-2038 is attached.	

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE _____ Date 3-21-03

TYPED or PRINTED NAME Gregory A. Hunt REGISTRATION NO. *(if appropriate)* 41,085

TELEPHONE 919-493-8000 Docket Number: 297/171

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S.D Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

60456775 .032103

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March 21, 2003

"Express Mail" mailing number.: EV281802265US
Date of Deposit: March 21, 2003
I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner for Patents, BOX PROVISIONAL APPLICATION, Washington, D.C. 20231.

Shaylor E. Dunn

Commissioner for Patents
BOX PROVISIONAL APPLICATION
Washington, D.C. 20231

Re: U.S. Provisional Patent Application for NANOSCALE PATTERNING BY MULTIPERIOD EDGE DEFINITION (SPACER GATE) LITHOGRAPHY FOR ELECTRONIC, PHOTONIC, MOLECULAR-ELECTRONIC, SPINTRONIC AND OTHER NANOTECHNOLOGY APPLICATIONS
Our File No. 297/171

Sir:

Please find enclosed the following:

1. A U.S. provisional patent application for NANOSCALE PATTERNING BY MULTIPERIOD EDGE DEFINITION (SPACER GATE) LITHOGRAPHY FOR ELECTRONIC, PHOTONIC, MOLECULAR-ELECTRONIC, SPINTRONIC AND OTHER NANOTECHNOLOGY APPLICATIONS (15 pages);

2. Provisional Application for Patent Cover Sheet (Form PTO/SB/16) in duplicate;

3. A return-receipt postcard to be returned to our offices with the U.S. Patent and Trademark Office date stamp thereon; and

4. A Certificate of Express Mail No.; EV281802265US.

Please contact our offices if there are any questions.

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account Number **50-0426**.

Respectfully submitted,

JENKINS & WILSON, P.A.

Gregory A. Hunt
Registration No. 41,085
Customer No. Bar Code Label:

25297
PATENT TRADEMARK OFFICE

GAH/sed

Enclosures

CONFIDENTIAL *(NCSU Patent Office Use Only)*
NCSU File No. _____
Lawyer's File No. _____

NCSU INVENTION DISCLOSURE FORM

This form must be signed by the Department Head and the College Dean/Associate Dean prior to submission.

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Social Security No:
Citizenship:
Department:
Telephone:

Inventor's Name:
Title:
Mailing Address:
Social Security No:
Citizenship:
Department:
Telephone:

1. Title of Invention: Nanoscale Patterning by Multiperiod Edge Definition (Spacer Gate) Lithography for Electronic, Photonic, Molecular-Electronic, Spintronic and other Nanotechnology Applications

2. Date Invention Conceived (Conception Date): _____

3. Has the Invention been reduced to practice? ☐ Yes No

4. Supporting Data Notebook No. Notebook Computer Files: Mark Johnson
Pages _____

5. Has the Invention been published: Orally No In writing No

   a. When: _____
   b. Authors: _____
   c. Any changes in the Invention since public disclosure (please attach copies of any publications, if available): _____

6. Brief Description. Is the Invention a new process, composition of matter, a device or one or more products? A new use for, or an improvement on an existing process. Please describe.
Invention is a process for the photolithographic patterning on the 1-100 nanometer spatial dimension as necessary for nanofabrication of materials and devices. This invention is a process which achieves nanometer scale pattern definition, which is beyond the optical limits imposed by the diffraction limited focusing requirements of photolithographic processes. The primary motivations and innovations in this disclosure are the use of multiple (2 or more) different materials (with differing selective etching or fabrication chemistries between the materials) in a process of edge definition lithography (also called 'spacer gate lithography') in the manufacturing process. The combination of multiple edge definition deposition/etchback sequences allows for two specific improvements: nanoscale patterning of 1D or 2D arrays of lithographically defined features with nanometer scale dimensions and the development of a sidewall etch reversal or lift-off process with nanometer scale dimensions. Application of this process enables a multitude of fabrication processes for the practical manufacturing of electronic, photonic, spintronic, molecular electronic or nano- mechanical systems. In addition to specific process invention claims, potential devices fabricated on the nanometer scale are also described. This process meets the fabrication requirements projected in the ITRS roadmap (Moore's Law.) for the 2009-2014 timeframe. [Additional Detailed Description Attached]

(Insert additional sheets to elaborate or attach descriptive material before page 4.)

7. Write a brief descriptive abstract of your Invention without making a disclosure. This will be used for marketing purposes.
This invention describes novel photolithography methods required to achieve nanoscale patterning of semiconductor materials and devices using conventional lithography equipment, and the incorporation of these processes device fabrication processes. Extension of lithographic methods to the nanometer spatial domain is a critical enabling technology for the practical realization of electronic (digital and RF/wireless), photonic, molecular-electronic, spintronic and nano-mechanical (NEMS) devices which have been proposed for this spatial scale.

8. From the description, pick out and expand on novel and unusual features. How does the Invention differ from present technology? What problems does it solve or what advantages does it possess?
1.) Use of edge definition lithography with multiple parallel features to achieve nanometer scale patterning with multiple parallel features. (Edge definition lithography has previously been used to define individual fetures in the nanometer spatial scale.) The ability to fabricate arrays of nanometer

scale features using conventional optical lithography will enable the practical realization of many proposed structures.
{Comparison: Current spacer gate technology employs a single material as a discrete feature which is usually linear and is not formed as an array}

2.) Use of edge definition lithography (spacer gate) for a reversal / lift-off process in nanometer scale patterning and fabrication of devices.
{Comparison: Current spacer gate technology is a positive image lithographic technique and has not been developed for image reversal (negative image) on the nanometer scale.}

3.) Use of two separate multiple array nanofabrication steps, with differing azimuthal orientations, to achieve a two-dimensional array of features which are non-linear in shape.
{Comparison: Current spacer gate technology generates individual or discrete features which are linear in shape.}

4.) Specific devices incorporating these processes are described. For electronic device fabrication, this spatial scale is consistent with the projected feature scale of the ITRS (Silicon technology roadmap) and hence may be the key technology for extending Moore's law in the 6-12 year time horizon. For molecular electronics, this spatial scale is consistent with the requisite interconnect distances of the active molecules. For photonic crystals, periodic arrays on this feature size is consistent with the formation of photonic bandgap materials in the visible and ultraviolet wavelength range.
{Comparison: For each of these devices, the availability of practical lithographic fabrication processes are currently key limiting factors and roadblocks in the achievement of technological advances. Improvement in device performance is necessary to achieve projected electronic system level goals. The improvements due to spatial scale reduction have been prediced and modeled throughout the industry. Our invention claim will be the use of multiperiod edge definition lithography to meet these devices fabrication requirements, and specific devices fabricated thereby.}

9. In not indicated previously, what are possible uses for the Invention? In addition to immediate applications are there other uses that might be realized in the future?
1.) Fabrication and integration of all semiconductor digital logic chips meeting Moore's Law requirements in the 6-12 year time horizon. (Full scale production in 2009-2015)
2.) Compound Semiconductor Devices (GaAs, InP, GaN, SiGe) with 1-100 nanometer scale gates for RF, microwave and mm-wave application. (Particularly X-band, K-Band and higher frequencies)
3.) Molecular electronic device interconnect technologies
4.) Visible, IR and UV photonic bandgap crystals (addressing current needs)
5.) Multiple nanoscale fabrication applications for organic and inorganic applications

10. Does the Invention possess disadvantages or limitations? Can they be overcome? How?
1.) Technology has yet to be demonstrated. [Laboratory demonstrations proposed and to proceed.]
2.) Throughput limitiations for lateral nanoscale array formation
(Optical feedback and automation approach to be applied.)
3.) Detailed control of nanoscale features required during deposition and etchback
(In-situ process control profile approach to be applied.)
4.) Detailed demonstration of overgrowth facets required for an image reversal and lift-off process with nanoscale resolution.

11. Enclose sketches, drawings, photographs and other materials that help illustrate the description. (Rough artwork, flow sheets, Polaroid photographs and penciled graphs are satisfactory as long as they tell a clear and understandable story.)
(Attached)

OTHER PERTINENT DATA

1. Is a publication or oral disclosure descriptive of the Invention planned within the next six months? Please give the date (estimate, if known) and attach copies of any existing manuscripts, preprints, abstracts or poster material. 1.) Scientific Publication of Technique and Results Planned
2.) Inclusion in SRC/MARCO Proposal Planned (May 2003)
3.) Inclusion in DARPA Molecular Electronics Proposal Planned (April 2003)

2. Is there an urgency in making a patent application? If so, please give the likelihood that similar technology may be developed elsewhere. Yes.
1.) Discrete Edge Defined (Spacer Gate) Lithography Actively Researched and Developed for nanoscale patterning by NCSU, Intel, SCR, SEMATECH, UC Berkeley and Elsewhere. Berkeley in particular is very active in researching and exploiting discrete spacer gate lithography concepts.
2.) Molecular Electronics actively developed by NCSU, Yale, Rice and elsewhere.
3.) Upcoming DARPA program on Molecular Electronics and SRC/MARCO program on semiconductor process research will require disclosure as part of application procedure.
4.) Technology has technical need, active research and high visibility (silicon ITRS roadmap, Moore's Law, etc.).
This technique, or similar, will likely be developed to fill the requirements of Moore's Law.

3. Have any graduate students and/or other technicians been involved in this research? No. At this point the research has only been discussed by faculty members during the preparation of upcoming research proposals.

If so, should the individual(s) be included as a co-inventor? N/A

4. Has the Invention been tested experimentally? Are experimental data or prototypes available?

5. Are there any prior applications for patent by the inventor on this subject? If so, give the serial number(s) and the filing date(s).
Johnson – None
Barlage -

6. Are there known inventions by other researchers that are related to this one? Please describe, including information on relevant patents and publications, if available.
Spacer Gate Technology – (UC. Berkeley)
Edge Definition Lithography – C. Osborne (NCSU)

7. Was the work that led to the Invention sponsored by industry or funded by State Federal appropriations? If so, attach a copy of the contract or agreement, if possible, and fill in the appropriate blanks below. One of the below MUST be completed. (This includes the source(s) of funds for the salary of each inventor.)

a. Complete Name of Government Agency: _____
Contract or Grant No. _____

b. Name of Industrial Company: _____

c. Name of Private Sponsor: _____

d. State or Federal Appropriation: State Salary and Start-Up Funds for Inventors (Idea Conception)

8. Has the Invention been disclosed to industry representatives? Has any commercial interest been shown in it? Please name companies; listing specific individuals and their titles if you know them.
None

a. Do you know of other companies that might be particularly interested in the Invention?
Every Manufacturer of semiconductor devices (Market >$100B Annually)
SRC, Sematech, Intel, Motorola, AMD, IBM, Cree, Nitronex, Applied Materials, AMSL, ASM, Lam Research, Micron Technologies, TI, TSMC, RF Micro Devices, Filtronics

b. List any manufacturers making comparable equipment or products.
Same as Above

c. How much do you estimate your Invention will cost to make?
Incremental Cost / Process Change in $1-$10B semiconductor fabrication plant
Throughput costs of multiple edge definition steps must be minimized.

Multiperiod Edge Definition Lithography

Background

The fabrication of semiconductor devices, as well as many other related high-technology products, requires the deposition and definition of materials with small dimensional features. The operation and performance capabilities of these devices are inversely related to the minimum spatial feature dimensions. Traditionally, the definition of small feature size is accomplished by photolithography. These photolithographic processes are limited to a minimum feature related to the wavelength of the light (or electrons) used in photolithography. The reduction in feature size necessary to meet the demands of, integrated circuit technology have challenge the limits of optical lithography necessitating the development of novel lithographic patterning methods including x-ray lithography, deep ultra-violet (DUV) lithography, electron-beam lithography and phase shift lithography. One approach for reducing the minimum feature size achievable with traditional optical lithography equipment is a process known as edge-definition lithography or spacer gate lithography. As described in figure 1, edge-definition lithography involves the isotropic deposition of a material (1-100 nm) over a lithographically defined block mask feature, and anisotropically etching of the deposited material and preferential etching of the block mask feature. This process results in a mask material which remains edge-on and for which the width corresponds to the thickness of the isotropically deposited layer (in the range of 1-100nm). This technique has been used to fabricate individual transistor devices which are <30nm in gate length as a demonstration of nanoscale transistors.

Many potential device technologies, including nanoelectronics, photonic crystals, spintronics, nano-electro mechanical systems (NEMS) and molecular electronics require the fabrication of periodic structures on the 1-100nm feature scale. As an example, proposed molecular electronics or carbon nanotube devices require an interconnection technology on the nanometer scale to enable the integration discrete devices. Integration of devices on an interconnect platform is one approach, and would require the fabrication of a host array by photolithography. As such, a photolithography method for fabricating an array of features with small interconnect spatial dimensions (1-100nm) is desired. This disclosure describes a fabrication method for edge defined lithographic arrays to meet such requirements. These arrays may have either a regular or varying periodicity, and may be patterned in 1 dimension or 2 dimensions.

Description of Invention

This invention is a process for photolithographically fabricating an array of nanometer scale features through the use of a overhanging pattern adjacent and connected to a traditionally defined lithographic feature. In addition to the process invention, possible or potential devices fabricated using this process are described. The list of devices are a subset of all possible devices fabricated using the techniques described. The initially preferred embodiment of this process is given graphically in figure 2:

1.) A block feature is defined using standard photolithographic techniques on a substrate for fabrication. The spatial dimensions of this feature may be consistent with the diffraction limited focusing conditions of standard or advanced photolithography techniques. (For example, this feature may be ~1μm by ~1μm in size.) The block feature may consist of photoresist, a metal, or an insulator. An attribute of this block feature is an etch chemistry consistent with subsequent differential removal of the block feature after array fabrication.

2.) A mask material (material 1) is deposited isotropically (or with a predictable and limited degree of anisotropy) across the masked surface feature and the substrate surface. In-situ process controls (optical measurements, piezoelectric QMS, etc.) or ex-situ process measurements (profilometry, optical measurements, Scanning microscopy, etc.) may be used to control or measure the deposited layer process and structure. The conditions for selection of material 1 include a differential etch chemistry relative to both the field mesa mask material from step 1 and the subsequently deposited material 2. Additional material selection criteria may be based on the necessity of either material 1 or material 2 persisting as a residual component of the subsequently fabricated device. (ie. It may need to have the properties of a gate metal for the fabricated circuit.) A detailed description of the first material deposition is shown in Figures 4a and 4b.

3.) The material 1 is anisotropically etched from the surface, leaving features which were initially adjacent to the masked area sidewall. The degree of anisotropy of the etch process must be greater than the anisotropy of the deposition process. The differential anisotropy results in a greater effective cross-section for material removal in the areas of the deposited sidewalls. The remaining material following the anisotropic etch is a patterned feature with a lateral dimension comparable to the thickness of the isotropically deposited material. A single sequence of isotropic deposition and anisotropic removal constitutes the prior art 'spacer-gate' technology as shown in figure 1. Subsequent fabrication steps include the differential removal of the lithographically defined block or mesa region material. The final structure fabricated thereby is a line of material which is defined to a 1-100nm spatial dimension. (A detailed description of the first material deposition is shown in Figures 4a and 4b.)

4.) The new process continues with a second material (material 2) which is deposited isotropically (or with a predictable and limited degree of anisotropy) across the masked surface feature (Including the material 1 spacer gate) and the substrate surface. In-situ

process controls (optical measurements, piezoelectric QMS, etc.) or ex-situ process measurements (profilometry, optical measurements, Scanning microscopy, etc.) may be used to control or measure the deposited layer process and structure. The conditions for selection of material 2 include a differential etch chemistry relative to both the field mesa mask material from step 1 and the deposited material 1 from steps 2 and 3. Depending on the specific device being fabricated, either material 1, material 2 or the field mask may need to be removed through differential etching. Additional material selection criteria may be based on the necessity of either material 1 or material 2 persisting as a residual component of the subsequently fabricated device. (ie. It may need to have the properties of a gate metal for the fabricated circuit.)

4.) The material 2 is anisotropically etched from the surface, leaving features which were initially adjacent to the masked area sidewall. The degree of anisotropy of the etch process must be greater than the anisotropy of the deposition process. The differential anisotropy results in a greater effective cross-section for material removal in the areas of the deposited sidewalls. The remaining material following the anisotropic etch is a patterned feature with a lateral dimension comparable to the thickness of the isotropically deposited material. While the single sequence of isotropic deposition and anisotropic removal constitutes the prior art 'spacer-gate' technology, the novel innovation is the subsequent deposition and removal of two (or more) different materials in conjunction with and as an extension of the initial spacer gate as shown in figures 2d and 2e. Subsequent fabrication steps include the differential removal of the lithographically defined block or mesa region material. The final structure fabricated thereby is a line of material which is defined to a 1-100nm spatial dimension.

Initial Claims:

1.) Process for multiperiod (2 or more) edge definition lithography at nanometer dimensional scale (1-100nm) using two or more spacer gate materials.
2.) Differential etching of materials following multiperiod edge definition lithography process.
3.) Multiperiod edge definition lithography with two or more materials in a regular array or irregular array geometry.
4.) Multiperiod edge definition lithography with two or more materials in a regular interlayer spacing or irregular interlayer spacing.
5.) Sequential (one or more sequences) multiperiod edge definition lithography processes with aligned or misaligned azimuthal orientation. Sequential processes result in one (1) dimensional, two (2) dimensional or three (3) dimensional arrays of nanometer scale features.
6.) Edge definition lithography using image reversal process to define nanometer dimensional scale (1-100nm) opening (gap) in a material.
7.) Bi-directional edge definition lithography to define a controlled, reduced spacing layer as small as zero (0) nanometers following image reversal process.
8.) Redeposition or regrowth of material in opening formed by image reversal process defined gap or whole.
9.) Specific devices fabricated using multiperiod edge definition lithography including transistors, integrated circuits, interconnect layers (1, 2 or 3 dimensional), molecular electron devices, spintronic devices, and photonic devices.
10.) Methods for in-situ and ex-situ control of deposition and etching processes during multiperiod edge definition lithography or lithography reversal based on optical, electrical, piezoelectric, magnetic or displacive measurements.

Claims

What is claimed is:

1. A method for forming a plurality of decananometer-spaced (5-100nm) channels in a substrate, the method comprising:
   (a) isotropically depositing a first mask material on a substrate having a first region at a first level and a second region at a second level higher than the first level;
   (b) anisotropically etching the first mask material from the substrate to produce a first sidewall extending from the substrate at an intersection of the first and second regions;
   (c) isotropically depositing on the substrate a second mask material different from the first mask material, the second mask material covering the first and second regions and the first sidewall;
   (d) anisotropically etching the second mask material from the substrate to produce a second sidewall adjacent to the first sidewall, the first and second sidewalls having pitches on the order of nanometers;
   (e) repeating steps (a)-(d) a predetermined number of times to produce a plurality of adjacent nanometer-pitched sidewalls alternatingly formed of the first and second mask materials;
   (f) selectively etching the second mask material from the substrate leaving the first sidewalls formed of the first mask material spaced from each other on the substrate by decananometer dimensions; and
   (g) etching regions of the substrate between the first sidewalls to form a plurality of decananometer-spaced channels in the substrate.

2. The method of claim 1 further comprising forming a plurality of decananometer-spaced structures in a substrate, where the spacing between structures is uniformly spaced and periodic.

3. The method of claim 1 further comprising forming a plurality of decananometer-spaced structures in a substrate, where the spacing between structures is non-uniform or non-periodic.

4. The method of claim 1 further comprising forming a plurality of decananometer-spaced structures in a substrate, where the thicknesses of the features are uniform equally spaced and of uniform thickness.

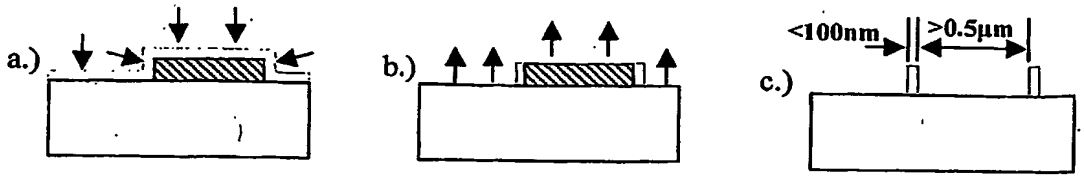
5. The method of claim 1 further comprising forming a plurality of decananometer-spaced structures in a substrate, where the thicknesses of the features are non-uniform and of unequal thickness.

6. A method for forming a decananometer-sized (5-100nm) channel in a substrate, the method comprising:
   (a) depositing a decananometer-pitched line of first mask material on a substrate;
   (b) anisotropically depositing a second mask material on the substrate, such that the second mask material covers the line of the first mask material with a first thickness, forms first and second sidewalls on first and second sides of the line with a second thickness being less than the first thickness, and covers the substrate in regions adjacent to the first and second sidewalls with the first thickness;
   (c) etching portions of the first and second sidewalls from the line of the first mask material;
   (d) removing the first mask material from the substrate leaving a channel in the second mask material having the same width as the line of first mask material; and
   (e) etching a channel in the substrate corresponding to the channel in the second mask material.

7. The method of claim 6 wherein depositing the first line on the substrate includes using steps (a)-(d) in claim 1.

8. The method of claim 6 wherein etching portions of the first and second sidewalls includes preferentially etching the first and second portions of the sidewalls such that the portions of the second material adjacent to the sidewalls and on top of the line of the first mask material are not removed.

Figure 1
Method of Edge Definition Lithography (Advanced Prior-Art Method)



Spacer gate method for nanoscale feature definition. a.) Isotropic deposition of a gate material over a field mesa patterned by traditional lithographic techniques; b.) anistropic etching of mask material. Sidewall areas have a higher cross-secction to anisotropic etching and are not completely removed; c.) Selective etch of initial field mesa leaving gate material with dimensions determined by isotropic deposition thickness.

Figure 2
Method of Linear Edge Definition Lithography Arrays (Innovative IP)

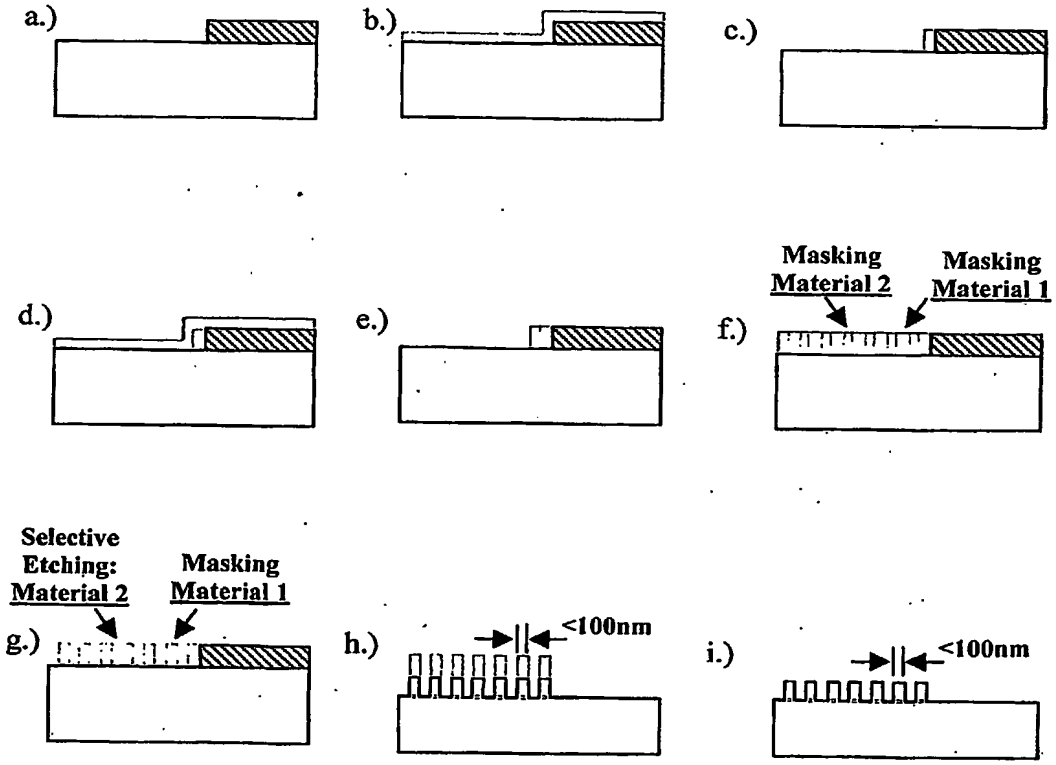


Figure 3

Linear (2-Dimensional) Array and Patterned (3-Dimensional) Array (2 Dimensional or Higher Dimensional Extension of Innovative IP)

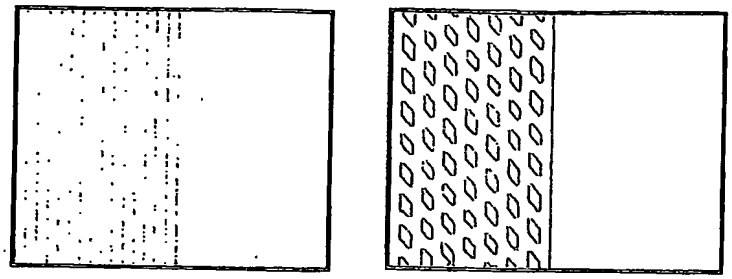


Figure 4
Isotropic Deposition and Anisotropic Etch/Removal of Material over Photographically Defined Mask Feature. Technique Sequence is Basis for Spacer Gate Process.

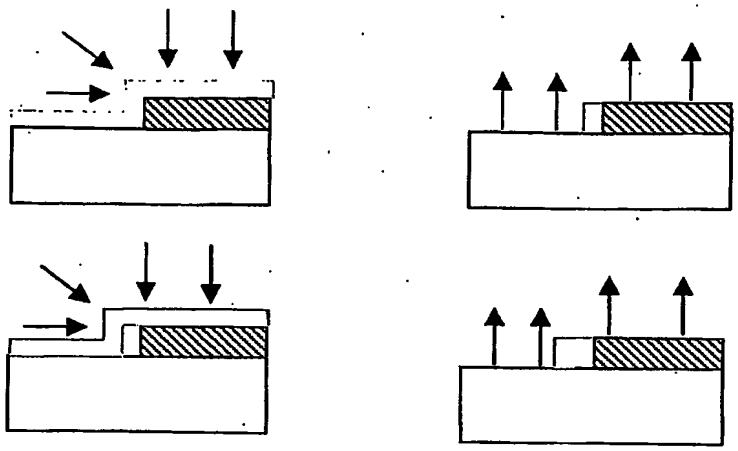


Figure 5

Anisotropic Deposition, Isotropic Etchback, and Lift-off Removal of Material over Photographically Defined Mask Feature with Nanometer Scale Features. (Technique is Basis for Spacer Gate Reversal Definition Process.)